AMENDMENTS TO THE CLAIMS:

Please amend claims 1, 8, 9-15, 23, 24, 27 and 28, as shown below.

This listing of claims will replace all prior versions and listings of claims in the Application:

Claim 1 (currently amended): A method of using a computer device for testing a mask pattern, the method comprising the steps of:

(a) applying optical proximity-effect compensation to a first pattern to be tested and to be formed onto a mask layer, to thereby actually form a mask pattern of said mask layer;

(b) dividing said first pattern into a plurality of areas in accordance with a second pattern to be formed onto another mask layer;

(c) determining sampling points on an edge of said first pattern;

(d) determining a test standard for each of said areas;

(e) simulating with a computer device a resist pattern formed on a resist by exposing said resist to a light through said mask pattern; and

(f) checking whether a dimensional gap between said first pattern and said resist pattern at each of said sampling points is within a test standard associated with an area to which each of said sampling points belongs,

wherein a test standard for a first area among said areas and a test standard for a second area among said areas are different from each other, wherein the quantity of sampling points on the edge of said first pattern in the first area is different than the quantity of sampling points on the edge of said first pattern in the second area[[.]]; and

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wherein said compensated mask pattern of said mask layer is generated by changing a condition of the proximity-effect compensation when a difference between said mask design pattern to be tested and said resist pattern is out of the test standard,

wherein a process is ended when the difference between said mask design pattern to be tested and said resist pattern is within the test standard.

Claim 2 (original): The method as set forth in claim 1, wherein a N-th sampling point located in a N-th area, among said sampling points, is determined in accordance with a N-th process in said step (c) wherein N indicates an integer equal to or greater than one (N = 1, 2, 3, 4, ---), and first to N-th processes are different from one another.

Claim 3 (original): The method as set forth in claim 1, further comprising:

dividing an edge of said first pattern into a plurality of portions, wherein said test standard is determined for each of said portions.

Claim 4 (original): The method as set forth in claim 1, wherein said first pattern is a pattern for forming a wiring layer, said second pattern is a pattern for forming a contact reaching said wiring layer, and said first area includes a third area including a contact area in which said contact makes contact with said wiring layer.

Claim 5 (original): The method as set forth in claim 4, wherein said third area is comprised of said contact area and an ambient area surrounding said contact area.

Claim 6 (original): The method as set forth in claim 1, wherein said first pattern is a pattern for forming a wiring layer including a gate of a MOS transistor, said second pattern is a pattern for forming an active area of said MOS transistor, and said first area includes a fourth area including a fifth area obtained by projecting said active area onto said first pattern.

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Claim 7 (original): The method as set forth in claim 6, wherein said fourth area is comprised of said fifth area and an ambient area surrounding said fifth area.

Claim 8 (currently amended): A non-transitory computer-readable medium storing a program for causing a computer to carry out a method of testing a mask pattern, wherein said method is executed by said computer in accordance with said program including the steps of:

(a) applying optical proximity-effect compensation to a first pattern to be tested and to be formed onto a mask layer, to thereby actually form a mask pattern of said mask layer;

(b) dividing said first pattern into a plurality of areas in accordance with a second pattern to be formed onto another mask layer;

(c) determining sampling points on an edge of said first pattern;

(d) determining a test standard for each of said areas;

(e) simulating a resist pattern formed on a resist by exposing said resist to a light through said mask pattern; and

(f) checking whether a dimensional gap between said first pattern and said resist pattern at each of said sampling points is within a test standard associated with an area to which each of said sampling points belongs,

wherein a test standard for a first area among said areas and a test standard for a second area among said areas are different from each other, wherein the quantity of sampling points on the edge of said first pattern in the first area is different than the quantity of sampling points on the edge of said first pattern in the second area[[.]]; and

wherein said compensated mask pattern of said mask layer is generated by changing a condition of the proximity-effect compensation when a difference between said mask design pattern to be tested and said resist pattern is out of the test standard,

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wherein a process is ended when the difference between said mask design pattern to be tested and said resist pattern is within the test standard.

Claim 9 (currently amended): The non-transitory computer-readable medium storing a program as set forth in claim 8, wherein a N-th sampling point located in a N-th area, among said sampling points, is determined in accordance with a N-th process in said step (c) wherein N indicates an integer equal to or greater than one (N = 1, 2, 3, 4, ---), and first to N-th processes are different from one another.

Claim 10 (currently amended): The non-transitory computer-readable medium storing a program as set forth in claim 8, wherein said steps further include:

dividing an edge of said first pattern into a plurality of portions, wherein said test standard is determined for each of said portions.

Claim 11 (currently amended): The non-transitory computer-readable medium storing a program as set forth in claim 8, wherein said first pattern is a pattern for forming a wiring layer, said second pattern is a pattern for forming a contact reaching said wiring layer, and said first area includes a third area including a contact area in which said contact makes contact with said wiring layer.

Claim 12 (currently amended): The non-transitory computer-readable medium storing a program as set forth in claim 11, wherein said third area is comprised of said contact area and an ambient area surrounding said contact area.

Claim 13 (currently amended): The non-transitory computer-readable medium storing a program as set forth in claim 8, wherein said first pattern is a pattern for forming a wiring layer including a gate of a MOS transistor, said second pattern is a pattern for forming an active area

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of said MOS transistor, and said first area includes a fourth area including a fifth area obtained by projecting said active area onto said first pattern.

Claim 14 (currently amended): The non-transitory computer-readable medium storing a program as set forth in claim 13, wherein said fourth area is comprised of said fifth area and an ambient area surrounding said fifth area.

Claim 15 (currently amended): A method of using a computer device for forming a mask having a desired mask pattern, the method including the steps of:

(a) applying optical proximity-effect compensation to a first pattern to be tested and to be formed onto a mask layer, to thereby actually form a mask pattern of said mask layer;

(b) dividing said first pattern into a plurality of areas in accordance with a second pattern to be formed onto another mask layer;

(c) determining sampling points on an edge of said first pattern;

(d) determining a test standard for each of said areas;

(e) simulating with a computer device a resist pattern formed on a resist by exposing said resist to a light through said mask pattern;

(f) checking whether a dimensional gap between said first pattern and said resist pattern at each of said sampling points is within a test standard associated with an area to which each of said sampling points belongs; and

(g) transferring said mask pattern onto a mask,

wherein a test standard for a first area among said areas and a test standard for a second area among said areas are different from each other, wherein the quantity of sampling points on the edge of said first pattern in the first area is different than the quantity of sampling points on the edge of said first pattern in the second area[[.]]; and

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wherein said compensated mask pattern of said mask layer is generated by changing a condition of the proximity-effect compensation when a difference between said mask design pattern to be tested and said resist pattern is out of the test standard,

wherein a process is ended when the difference between said mask design pattern to be tested and said resist pattern is within the test standard.

Claim 16 (original): The method as set forth in claim 15, wherein a N-th sampling point located in a N-th area, among said sampling points, is determined in accordance with a N-th process in said step (c) wherein N indicates an integer equal to or greater than one (N = 1, 2, 3, 4, ---), and first to N-th processes are different from one another.

Claim 17 (original): The method as set forth in claim 15, further comprising:

dividing an edge of said first pattern into a plurality of portions, wherein said test standard is determined for each of said portions.

Claim 18 (original): The method as set forth in claim 15, wherein said first pattern is a pattern for forming a wiring layer, said second pattern is a pattern for forming a contact reaching said wiring layer, and said first area includes a third area including a contact area in which said contact makes contact with said wiring layer.

Claim 19 (original): The method as set forth in claim 18, wherein said third area is comprised of said contact area and an ambient area surrounding said contact area.

Claim 20 (original): The method as set forth in claim 15, wherein said first pattern is a pattern for forming a wiring layer including a gate of a MOS transistor, said second pattern is a pattern for forming an active area of said MOS transistor, and said first area includes a fourth area including a fifth area obtained by projecting said active area onto said first pattern.

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Claim 21 (previously presented): The method as set forth in claim 1, wherein said mask layer to be tested is a gate layer, and a number of sampling points in an area acting as a gate of a transistor is higher than the same in other areas.

Claim 22 (previously presented): The method as set forth in claim 1, wherein said mask layer to be tested is a gate layer, and a number of sampling points in a contact area is higher than the same in other areas.

Claim 23 (currently amended): The non-transitory computer-readable medium storing a program as set forth in claim 8, wherein said mask layer to be tested is a gate layer, and a number of sampling points in an area acting as a gate of a transistor is higher than the same in other areas.

Claim 24 (currently amended): The non-transitory computer-readable medium storing a program as set forth in claim 8, wherein said mask layer to be tested is a gate layer, and a number of sampling points in a contact area is higher than the same in other areas.

Claim 25 (previously presented): The method as set forth in claim 15, wherein said mask layer to be tested is a gate layer, and a number of sampling points in an area acting as a gate of a transistor is higher than the same in other areas.

Claim 26 (previously presented): The method as set forth in claim 15, wherein said mask layer to be tested is a gate layer, and a number of sampling points in a contact area is higher than the same in other areas.

Claim 27 (currently amended): A computer device for testing a mask pattern performing the steps of:

(a) applying optical proximity-effect compensation to a first pattern to be tested and to be formed onto a mask layer, to thereby actually form a mask pattern of said mask layer;

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(b) dividing said first pattern into a plurality of areas in accordance with a second pattern to be formed onto another mask layer;

(c) determining sampling points on an edge of said first pattern;

(d) determining a test standard for each of said areas;

(e) simulating a resist pattern formed on a resist by exposing said resist to a light through said mask pattern; and

(f) checking whether a dimensional gap between said first pattern and said resist pattern at each of said sampling points is within a test standard associated with an area to which each of said sampling points belongs,

wherein a test standard for a first area among said areas and a test standard for a second area among said areas are different from each other, wherein the quantity of sampling points on the edge of said first pattern in the first area is different than the quantity of sampling points on the edge of said first pattern in the second area[[.]]; and

wherein said compensated mask pattern of said mask layer is generated by changing a condition of the proximity-effect compensation when a difference between said mask design pattern to be tested and said resist pattern is out of the test standard,

wherein a process is ended when the difference between said mask design pattern to be tested and said resist pattern is within the test standard.

Claim 28 (currently amended): A computer device for forming a mask having a desired mask pattern, the computer device performing the steps of:

(a) applying optical proximity-effect compensation to a first pattern to be tested and to be formed onto a mask layer, to thereby actually form a mask pattern of said mask layer;

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(b) dividing said first pattern into a plurality of areas in accordance with a second pattern to be formed onto another mask layer;

(c) determining sampling points on an edge of said first pattern;

(d) determining a test standard for each of said areas;

(e) simulating a resist pattern formed on a resist by exposing said resist to a light through said mask pattern;

(f) checking whether a dimensional gap between said first pattern and said resist pattern at each of said sampling points is within a test standard associated with an area to which each of said sampling points belongs; and

(g) transferring said mask pattern onto a mask,

wherein a test standard for a first area among said areas and a test standard for a second area among said areas are different from each other, wherein the quantity of sampling points on the edge of said first pattern in the first area is different than the quantity of sampling points on the edge of said first pattern in the second area[[.]]; and

wherein said compensated mask pattern of said mask layer is generated by changing a condition of the proximity-effect compensation when a difference between said mask design pattern to be tested and said resist pattern is out of the test standard,

wherein a process is ended when the difference between said mask design pattern to be tested and said resist pattern is within the test standard.

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